Please kindly amend the claims as indicated below.

1. (Amended Thrice) A system for responding to requests, said system comprising:

a requesting node for transmitting a request;

a responding node for transmitting a response to the request; and

~~logic operable to:~~

~~receive a signal from the requesting node indicating the presence of the request;~~

~~receive a signal from the responding node indicating the presence of data;~~

~~said~~ logic for ~~selectively~~ transmitting a signal to the requesting node indicating the presence of the response ~~based on amount of time elapsed between receiving the signal from the requesting node and receiving a signal from the responding node indicating the presence of data amount of time elapsed between receiving the signal from the requesting node and receiving the signal from the responding node is less than a predetermined amount of time~~, said logic receiving a signal from the responding node indicating the presence of data and a signal from the requesting node indicating the presence of the request, wherein the logic further comprises:

an AND gate for transmitting the signal to the memory controller after a time interval, wherein during the time interval, the AND gate receives the signal from the requesting node and the signal from the responding node.

2. (Amended Thrice) A circuit for transferring data, said circuit comprising:

a memory controller for issuing a read command to read the data;

a memory module for storing the data; and

logic for transmitting a signal to the memory controller causing the memory controller to receive the data, ~~if the logic receives a signal from the memory module indicating the presence of data within a predetermined period of time after receiving a signal from the memory controller indicating the presence of the request~~ said logic receiving a signal from the memory module indicating the presence of the data and a signal from the memory controller indicating the presence of the read command, wherein the logic further comprises:

an AND gate for transmitting the signal to the memory controller after a time interval, wherein during the time interval, the AND gate receives the signal from the memory controller and the signal from the memory module.

Claim 3 was cancelled without prejudice.

4. (Original) The circuit of claim 2, wherein the memory controller further comprises:

a sequencer core for issuing the read command; and

a queue for receiving the data.

Claim 5 is cancelled without prejudice.

6. (Original) The circuit of claim [5] 2, wherein the logic further comprises:

numerically controlled delay logic for receiving the read command, and for transmitting the signal indicating

the presence of the read command after a first predetermined period of time after receiving the read command.

7. (Original) The circuit of claim [5] 2, wherein the logic further comprises:

numerically controlled delay logic for receiving the read command, and for transmitting a first signal after a first predetermined period of time after receiving the read command and transmitting a second signal after a second predetermined period of time after receiving the read command; and

an OR gate for transmitting the signal indicating the presence of a read transaction, wherein the OR gate further comprises:

a first input for receiving the first signal; and

a second input for receiving the second signal; and

wherein the AND gate receives the signal from the memory controller directly and the signal from the memory module directly and transmits the signal to the memory controller directly.

8. (Original) The circuit of claim 7, wherein the memory module transmits the signal indicating the presence of the data between transmission of the first signal and transmission of the second signal.

9. (Original) The circuit of claim 7, wherein the memory module transmits the signal indicating the presence of the data between transmission of the rising edge of the

first signal and the transmission of the falling edge of the second signal.

10. (Original) The circuit of claim 2, wherein the memory module is a DDR-SDRAM.

Claims 11-16 are withdrawn.

17. (Amended Twice) A circuit for transferring from memory, said circuit comprising:

a memory controller, wherein the memory controller is operable to transmit a read request;

a memory module, wherein the memory module is operable to transmit data and a signal indicating transmission of the data;

logic connected to the memory controller, wherein the logic is operable to transmit another signal to the memory controller indicating the transmission of the data if the ~~logic received a signal from the memory module indicating the presence of data within a predetermined period of time after receiving a signal from the memory controller indicating the presence of the request~~, wherein the logic further comprises:

an AND gate connected to the memory controller, said AND gate operable to transmit the another signal to the memory controller after a time interval, wherein during the time interval, the AND gate receives the signal from the memory controller and the signal from the memory module; and

a printed circuit board connected to the memory controller, the memory module, and the logic, wherein the

printed circuit board is connected to transmit the read request to the memory module, and the signal indicating transmission of the data from the memory module to the logic.

18. (Original) The circuit of claim 17, wherein the logic further comprises:

a first numerically controlled delay logic;

a second numerically controlled delay logic connected to the first numerically controlled delay logic;

an OR gate connected to the first numerically controlled delay logic and the second numerically controlled delay logic and connected to the AND gate[; and

an AND gate connected to the OR gate and connected to the second printed circuit].

19. (Original) The circuit of claim 18, wherein the first numerically controlled delay logic controls a rising edge of a gating signal and wherein the second numerically controlled delay logic controls the falling edge of the gating signal.

20. (Original) The circuit of claim 17, wherein the memory controller further comprises:

a sequencer core connected to the logic and the first printed circuit; and

a queue connected to the logic to receive the another signal indicating the transmission of the data.

Please add the following claim.

--21. (New) The circuit of claim 1, wherein the AND gate receives the signal from the requesting node directly and the signal from the responding node directly, and wherein the AND gate transmits the signal to the memory controller directly.--